WHAT IS CLAIMED IS:

1. A method for testing a multi-chip package in order to test for intermittent or permanent short circuits in the internal components comprising the steps of:

(a) applying a rising temperature to the device under test while concurrently measuring the power bus to ground resistance during an up temperature ramp;

(b) incrementally reducing down the temperature of said device under test back to starting room temperature while monitoring and reading the power bus to ground resistance of the device;

(c) plotting a graph of the power bus to ground resistance of the device during the temperature up ramp and during the temperature down ramp.

2. The method of claim 1 which includes the step of:

(d) noting the regularity or irregularity of the up ramp and down ramp temperature graphs plotted against the power bus to ground resistance in order to determine the operability of components within the multi-chip package.

3. A method for t sting int rnal compon nts of an integrated circuit package having an internal power bus, said method comprising the steps of:

(a) cycling the ambient temperature around said integrated circuit package from room temperature up to a higher selected temperature and then back again to room temperature;

(b) reading out the power bus-ground resistance at selected intervals during the up-ramp temperature change and during the down-ramp temperature change;

(c) plotting a graph of the power bus-ground resistance against temperature during the up-ramp and down-ramp temperature change.

(d) observing the plotted graph to discern a substantially linear resistance change to indicate a normal operating set of components in the integrated circuit package.

4. The m thod of claim 3 wh r in st p (d) includ s the step of:

(d1) observing an erratic characteristic of the plotted graph to indicate an inoperative component that is shorted or open-circuited.

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5. The method of claim 3 wherein step B includes the step of:

(b1) controlling a Peltier-junction module to act as an increasing heat source or as a decreasing heat sink.

6. A method for t sting th integrity of internal components of an integrated circuit package having an internal power bus, comprising the steps of:

(a) setting a metallic transfer block unit at a normal room temperature;

(b) attaching a device under test to said transfer block and connecting said power bus-to ground connections internal connections of said device under test to a digital multimeter;

(c) utilizing a computer program for sequencing the temperature of said device under test into an upward temperature rise and subsequently into a downward temperature drop back to room temperature, while concurrently reading the power bus-to ground resistance every 2 seconds during the up-ramp cycle and the down-ramp cycle;

(d) plotting, on a computer screen, the said resistance readings during the up-ramp temperature cycle and the down-ramp temperature cycle;

(e) reading the plotted graph on said computer screen of the power bus-to ground resistance against the temperature up-ramp and down-ramp cycles in order to differentiate a normal set of workable components in said integrated circuit package in order to differentiate inoperable open-circuited or short-circuited components within said integrated circuit module.

7. An apparatus for testing internal components of an integrated circuit package, having an internal power bus, to determine normal operation or problem areas in said components, comprising:

(a) means for temperature cycling said package over a range of 20 degrees Celsius without opening up said package;

(b) means for logging a graph of said power bus to ground resistance against the temperature during the temperature cycle;

(c) means for analyzing said graph to determine normal operation or problem areas in said package.

8. The apparatus of claim 7 wherein said means for temperature cycling includes:

(a1) a computer generated sequencing program to control a Peltier thermoelectric module to act as a heat source and/or heat sink to said package under test.

9. The apparatus of claim 8 wherein said means for logging includes:

(b1) a computer program which graphs and logs the temperature and power bus to ground resistance every 2 seconds during the temperature cycling of said package under test.

10. An apparatus for testing internal components of an integrated circuit packaged device under test to determine normal operation or problem areas in the components, said apparatus comprising:

(a) test socket means for connecting the device under test with a digital multimeter in order to measure the power bus-to ground resistance of the internal components;

(b) temperature transfer block means connected to a temperature meter for placement adjacent said device under test in order to increase the ambient heat or decrease the ambient heat to said device under test;

(c) a Peltier-thermal electric module adjunct said transfer block means and connected to a programmable power supply for controlling the addition of heat to or reduction of heat from said temperature transfer block;

(d) heat sink and fan means placed adjunct to said Peltier thermal electric module and connected to a controlled fan power supply;

(e) computer means having a control program for connection and management of said controlled fan power supply, said programmable power supply and for sensing operations of said temperature meter and said digital multimeter to controllably enable the sequencing of an up-ramp temperature and a down ramp temperature adjacent said device under test, while concurrently reading-out and plotting the power bus-to ground voltage during the up-cycle and down-cycle of the temperature applied to said device under test.